New Error Amplifier Topology for Low Dropout Voltage Regulators Using Compound OTA-OPAMP

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Abstract— **Typical Low Dropout Voltage regulators (LDO), uses an error amplifier in a linear closed loop. The main advantage of such linear regulators is the low standby current due to the absence of switching. In addition, a fully integrated linear regulator with no external components is very attractive for applications with stringent area, low weight requirements and relatively small peak power.**

The architecture of error amplifier used in the feedback loop suffers from an inherent load regulation performance limitation. This limitation manifests itself through the limited DC open-loop gain, and results from limited closed-loop bandwidth. The frequency response of power supply loop is highly sensitive to the load conditions, thus, making proper compensation is a laborious effort. This paper discusses and addresses a new topology of an error amplifier offering a high open loop gain as well as a large band width by adding a zero to its transfer function. Proposed topology uses a compound OTA and OPAMP that enhances load regulation performance by relaxing the dc open-loop gain restrictions. An example of battery charger using this OpAmp topology is also described in this paper. This battery charger can be used as an LDO once the battery is not connected.

I. INTRODUCTION

The explosive proliferation of battery powered equipment in the past decade has accelerated the development and usage of power management blocks. The low-dropout voltage regulator (LDO) has slowly come in front of the linear ICs. The reduced input voltage requirement of an LDO is advantageous in battery powered systems, since it translates directly into fewer battery cells, less wasted power, smaller size, and lower cost.

Compared with switching regulators, the LDOs are less expensive, smaller in area and easier to be used. Moreover, the noise of output voltage is lower and the response to input voltage transient and output load transient is faster. These advantages make LDOs suitable for battery-powered equipments, communication systems, portable systems, and post regulators of switching regulators. Among possible process technologies, CMOS is very attractive for LDO circuit implementation because of its low cost, low power consumption and potential for system-on-chip integration. However, the LDO's performance requires the use of external compensation capacitors, which must be carefully selected to assure stability.

II. CONVENTIONAL LDO TOPOLOGIES

Conventional LDO regulator uses PMOS as a pass element to improve dropout voltage performance without increasing complexity of the circuit. Therefore, an LDO can be considered as a two-stage amplifier connected in a feedback loop [1]. The first stage is the so called "error amplifier" it consists on an Operational Transconductance Amplifier (OTA) having high output impedance. The second stage consists of a pass element connected as a common source stage. The load impedance is represented as a resistance R_L in parallel with a capacitor C_L and corresponding equivalent series resistance R_{ESR} (Fig. 1).

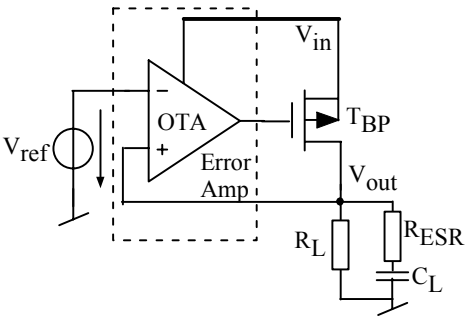

Figure.1 Conventional LDO structure.

Due to the high output resistance of the OTA (R_{OTA}) and the large load capacitance C_L, there is one pole at the output of each stage. Conventionally, the equivalent series resistance R_{ESR} is used to insert a zero between two low frequency poles and unity gain frequency [6]. Therefore, the output node of an LDO regulator is typically the drain of a PMOS power transistor and the dropout voltage required in this configuration is the overdrive voltage required to keep the PMOS transistor in saturation region. The price paid for the reduction in dropout voltage is the potential instability of the regulator. The impedance seen from the drain of the pass transistor is high and is inversely proportional to the load current. Hence, the pole at the drain of the pass transistor is heavily dependent on the load condition. The load current can range from few microamperes to amperes (in this paper the output current is $I_{Load,max}$= 1.38 A).

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A closed loop of a typical LDO voltage regulator (Fig. 1) reveals the fact that there are two low-frequency poles that need to be taken into consideration in evaluating the frequency response of the LDO's closed-loop transfer function. One of the poles lies at the output of the regulator and inversely proportional to the load impedance $P_1 \sim 1/Z_L$ (Z_L is composed by R_L, C_L and R_{ESR}), the other pole $P_2 \sim 1/(R_{OTA}.C_{TBP})$ is located at the gate of the pass transistor. Owing to the large size of the pass transistor (W=123'000µm, L=1.8µm in the design presented in this paper for an output current of I=1.38 A) and therefore, its huge input capacitance ($C_{TBP} \approx 0.6$ nF) together with the high output impedance of the error amplifier, the pole at its gate is located at low frequencies. There are, additional parasitic poles present in the LDO regulator. In fact, the error amplifier itself contributes as well with its internal parasitical poles. The system is therefore potentially unstable. A solution to this problem is to introduce a zero that compensates the phase contribution of one pole in order to guarantee a phase margin better than 45 degrees. In a conventional LDO voltage regulator, the electrostatic resistance R_{ESR} of the load capacitor generates this zero [10, 11].

The conventional phase compensation scheme using ESR compensation has several drawbacks. The ESR of a capacitor is not properly specified in many cases and varies with temperature. The high-frequency bypass capacitors placed in parallel with the output capacitor form a pole with the ESR of the output capacitor further decreasing the phase margin. Moreover, the user is permitted to use ESR usually in the range of 0.05–10 Ω [7, 11, 10]. On the other hand, the ESR compensation increases the overshoot drastically if large resistors are used.

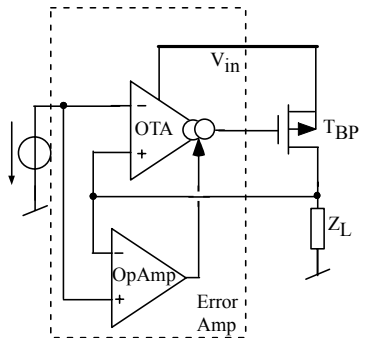

Figure.2 Proposed error amplifier structure.

Another proposed solution to the problem of LDO stability is to use pole-splitting techniques with the Miller capacitor across the gate and drain of the pass transistor [4, 10] to have a single dominant pole at any load. The Miller capacitor must be huge to push the LDO output pole beyond the unity gain frequency. Also, the Miller capacitor, along with the PMOS pass transistor, provides a direct path for the power supply spikes to reach the output. Therefore, the circuit has to be modified to have an extra buffer stage and this modification introduces additional parasitic poles [1]. A common-drawback of Miller compensation is that the pole of the first stage is pushed to low frequencies while the pole at the LDO output goes to higher frequencies.

III. PROPOSED CIRCUIT TOPOLOGY

Adding a zero to the transfer function of an LDO is one of the most frequently proposed solutions for the stability behavior. The error amplifier has to be stabilized by removing the effect of the variable pole at the output. This can be done via pole-splitting using compensation capacitors or pole-zero cancellation using feed-forward paths [2, 6]. Low-frequency pole-zero doublets can appear if the feed forward path does not cancel the pole properly, which may eventually cause the amplifier to be unstable.

The load regulation of an LDO is inversely proportional to the open loop gain of the error amplifier. On one side, good load regulation is generally reached if the error amplifier is realized by a two stage Operational Amplifier (OpAmp) topology instead of an Operational Transconductance Amplifier (OTA) structure. On the other side, the Unity Gain Frequency (UGF) of the error amplifier should be as high as possible. This requirement implies that an OTA should be used as error amplifier. In the proposed solution, the error amplifier will be realized by a compound OTA-OpAmp in order to achieve both requirements simultaneously:

- the OTA topology will provide a large bandwidth with a limited open loop gain.
- the OpAmp topology will provide a high DC gain to the overall loop improving thus the load regulation.

Fig. 2 depicts the proposed topology where an additional high gain OpAmp is added to the basic topology of fig. 1. The purpose of this OpAmp is to achieve a current boosting of the OTA output current. The inputs of both the OTA and the OpAmp are connected together where the OTA achieve a low gain large bandwidth while the OpAmp is designed to realize a high gain limited band-width.

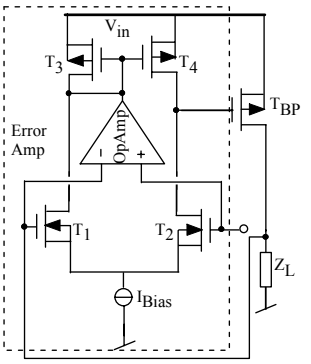

Figure.3 LDO scheme using compound OTA-OpAmp error amplifier.

Fig. 3 shows a possible implementation of the proposed compound OTA-OpAmp error amplifier [12]. The transistors T1, T2, T3 and T4 are used to implement a basic OTA topology biased by I_{Bias}. An additional two stage OpAmp is

added to boost the output current and improve the DC gain of the overall structure. The main advantage of this error amplifier is that, the main loop constituted by an OTA and the pass element is comparable to the classical topology of a basic LDO. The additional OpAmp will see as load the diode connected device T_3 which is almost constant and independent from the output load Z_L. Therefore the DC gain of this compound structure is mainly realized by the OpAmp, once the unity gain frequency of the LDO is the one achieved by the OTA.

IV. CIRCUIT IMPLEMENTATION

This error amplifier has been realized and implemented. Fig. 4 shows its transistor level scheme.

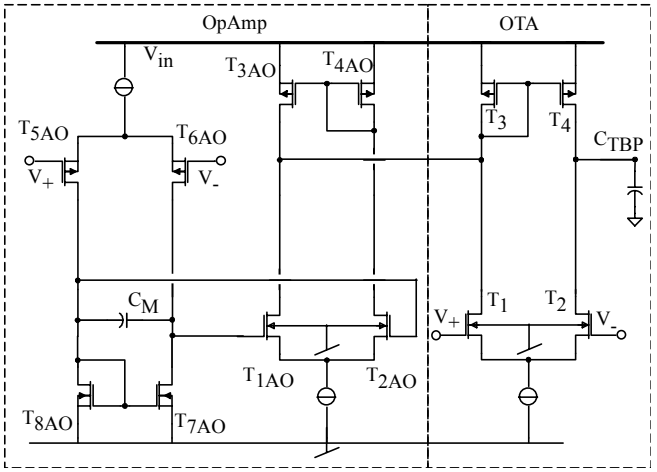

Figure.4 Error amplifier implementation.

The open loop gain A_{OpAmp} and the dominant pole f_{P1} of the two stage operational amplifier are:

$$A_{OpAmp} \approx \frac{g_{m5,6AO}}{g_{ds6AO}+g_{ds7AO}} \cdot \frac{g_{m1,2AO}}{g_{m3}} \quad \text{and} \quad f_{P1} \approx \frac{(g_{ds,6AO}+g_{ds,7AO})^2}{2\pi C_M g_{m5,6AO}}$$

With C_M being a Miller capacitor, its value is multiplied by the DC gain of the first stage of the OpAmp creating therefore a low frequency dominant pole.

The open loop gain A_{OTA} and the dominant pole f_{P2} of the OTA are:

$$A_{OTA} = g_{m_{1,2}} R_{OTA}\ ,\ f_{P2} \approx \frac{1}{2\pi C_{TBP} R_{OTA}} \text{ with } R_{OTA} = \frac{1}{g_{ds4}+g_{ds2}}$$

The DC gain of the error amplifier is: $A_0 = A_{OpAMp}.A_{OTA}$

The transfer function of the compound structure is depicted in the fig. 5. The location of the added zero is the same as the gain band width product GBW_{OpAmp} of the OpAmp.

$$f_Z = f_{GBW_{OpAmp}} \approx A_{OpAmp}.f_{P1} = \frac{g_{m1,2AO}.(g_{ds6AO}+g_{ds7AO})}{2\pi C_M.g_{m3}}$$

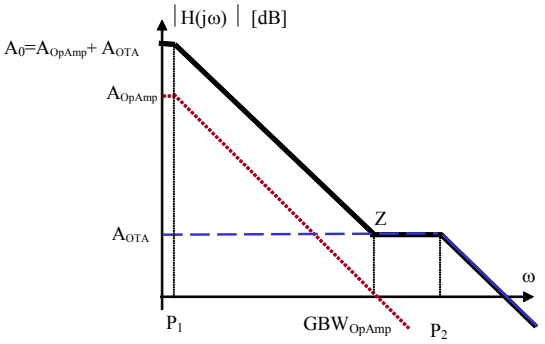

Figure.5 Bode plot of error amplifier.

V. BATTERY CHARGER USING COMPOUND ERROR AMPLIFIER

This compound error amplifier has been used in a battery charger system. The designed system should be able to be used as an LDO linear regulator once the battery is not connected [13]. In the fig. 6 the LDO subsystem is shown where an additional output current sensing function is provided. The microphotography of the overall battery charger system is shown on fig. 7 where the error amplifiers as well as the pass element are highlighted. A 0.8µm high voltage technology has been used in this implementation.

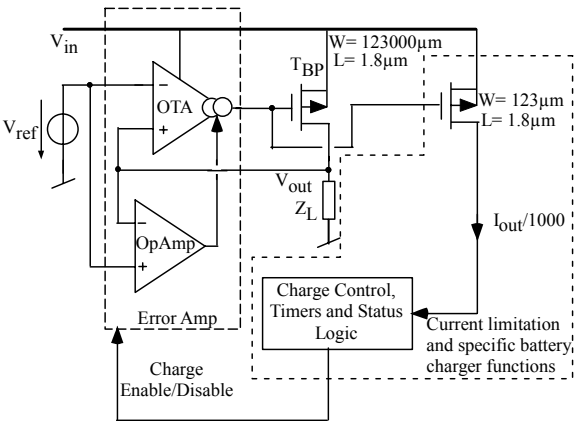

Figure.6 Battery charger: synoptic topology.

Table.I Performance parameters

	Measured Results
Vin	4.5V to 16 V
Vout	4.2 V
Quiescent current	300 µA
Dropout Voltage	300mV (I_{Load}= 1A)
Load Regulation	Typ : 0.01%, max: 0.25%
Line Regulation	Typ : 0.025%/V, max: 0.25%/V
Capacitor range	Max: 50 µF

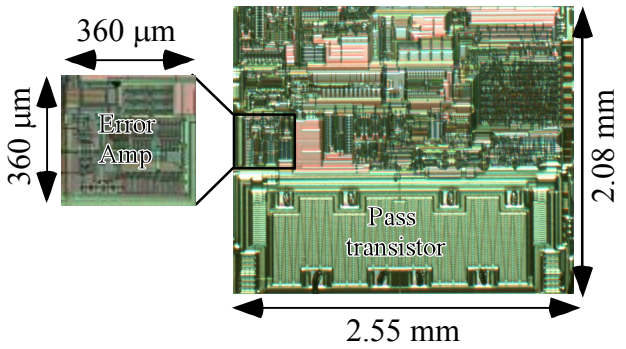

Figure.7 Microphotography of a complete battery charger system using the proposed error amplifier.

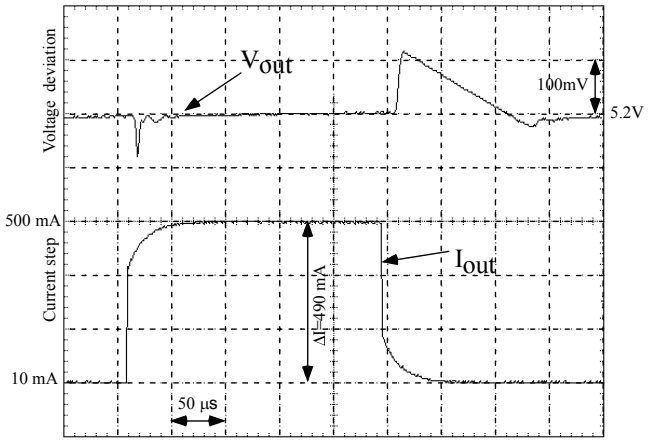

Figure.8 Load transient response measurement with a ceramic capacitor of 10 µF.

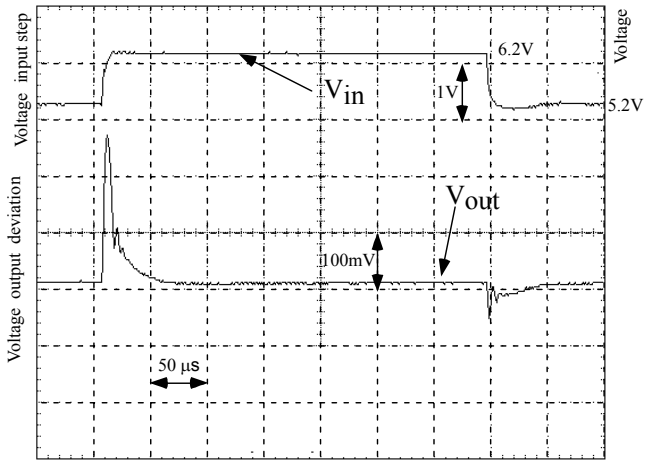

Figure.9 Line transient stepped from 5.2V to 6.2V with a ceramic capacitor load of 10 µF and an output current of 1A.

VI. CONCLUSION

In this paper the conventional scheme for LDO regulator is analyzed. A new technique using pole-zero pairs cancellation is introduced to improve the stability of the LDO function. This technique uses a basic OTA topology with output current boosting achieved by a two stages operational amplifier topology. The realized error amplifier has a large unity gain frequency and high DC open loop gain. An application of battery charger using this topology as LDO once the battery is not connected is described and performances results are presented.

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